

FIG 1

The diagram illustrates a multi-channel signal processing system with four parallel channels labeled 0, 1, 30, and 31. Each channel has its own input (Din0, Din1, Din30, Din31) and output (Dout0, Dout3). The system is organized into two main sections: a top section for channels 0 and 1, and a bottom section for channels 30 and 31, separated by a dashed line labeled 'LM' (likely representing a memory or logic block). Each channel section contains an address multiplexer (AMUX), a selection multiplexer (SM), a block processing unit (BPC), and a data multiplexer (Dmux). The top section also includes a vertical selection unit (VST) and a block processing unit (BPMUX). The bottom section includes a vertical selection unit (VST) and a block processing unit (BPMUX). The system is controlled by a common selection signal (SELECTION) and a common address signal (Adr.0 to Adr.3). The outputs of the channels are combined into a single output stream (Dout0 to Dout3) through a series of multiplexers (RKMUX0, RKMUX3) and a final output multiplexer (RKT). The system is designed to process multiple channels of data in parallel, with each channel having its own dedicated processing units and multiplexers.

FIG 2

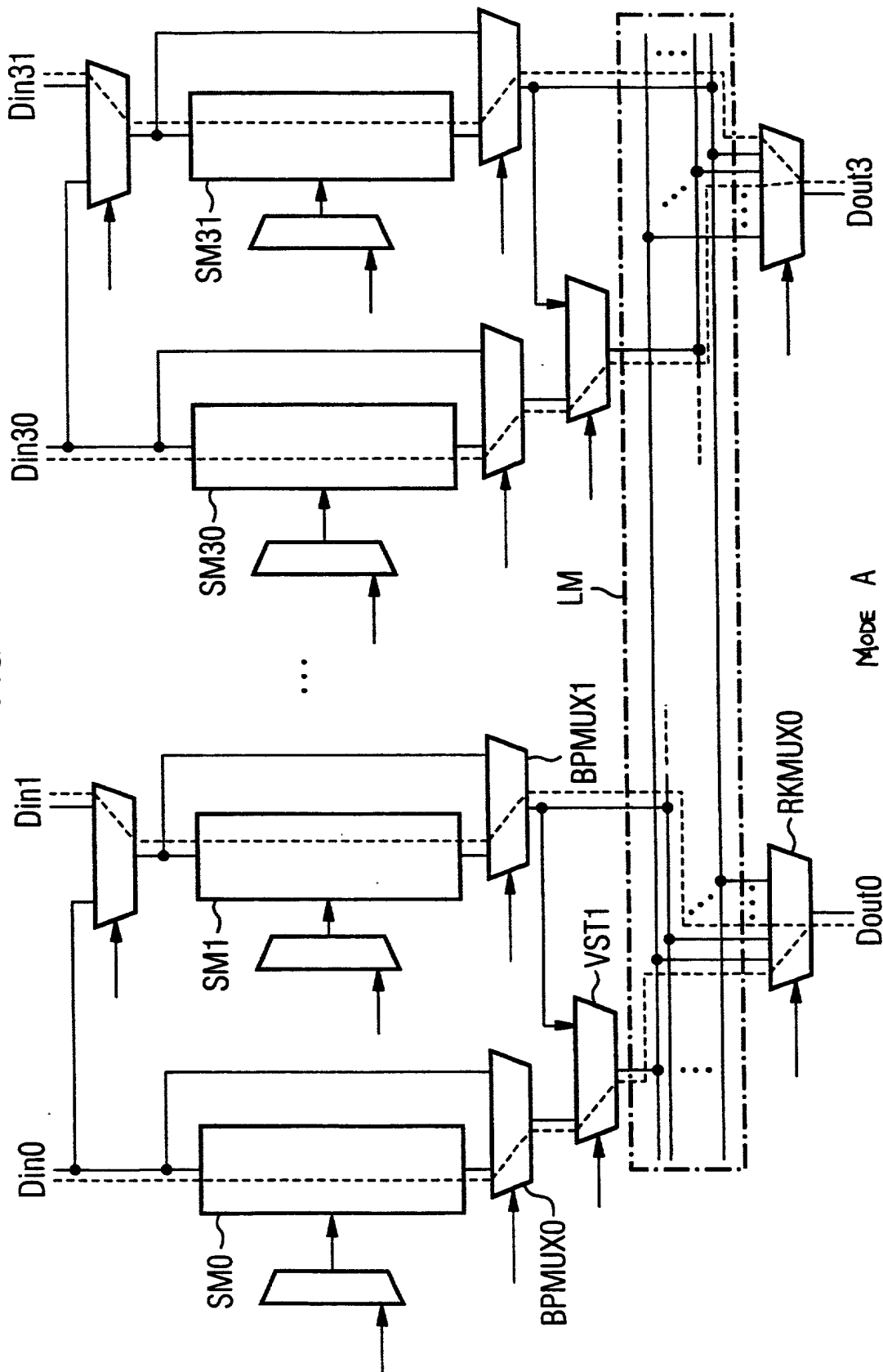


FIG 3

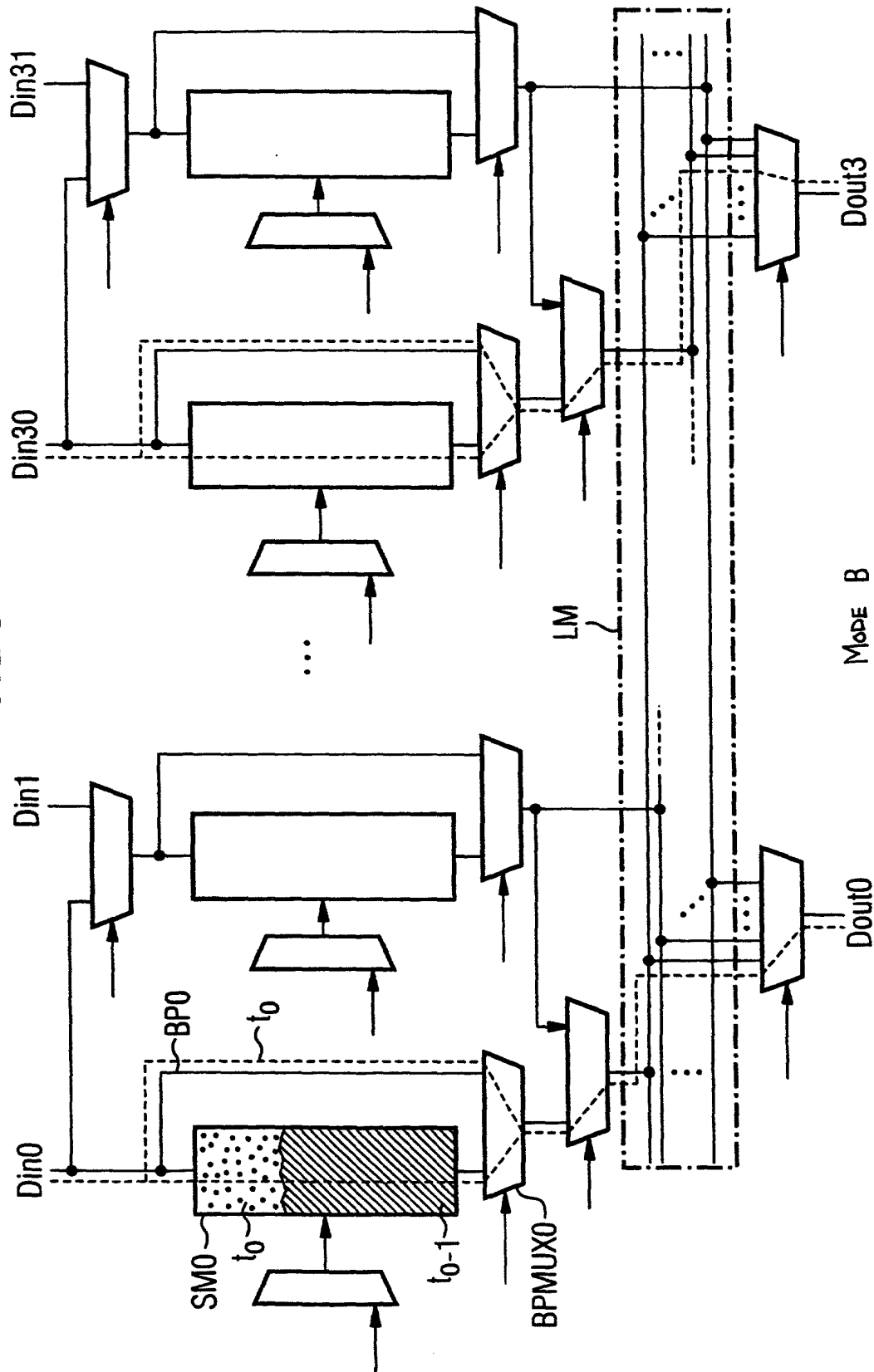
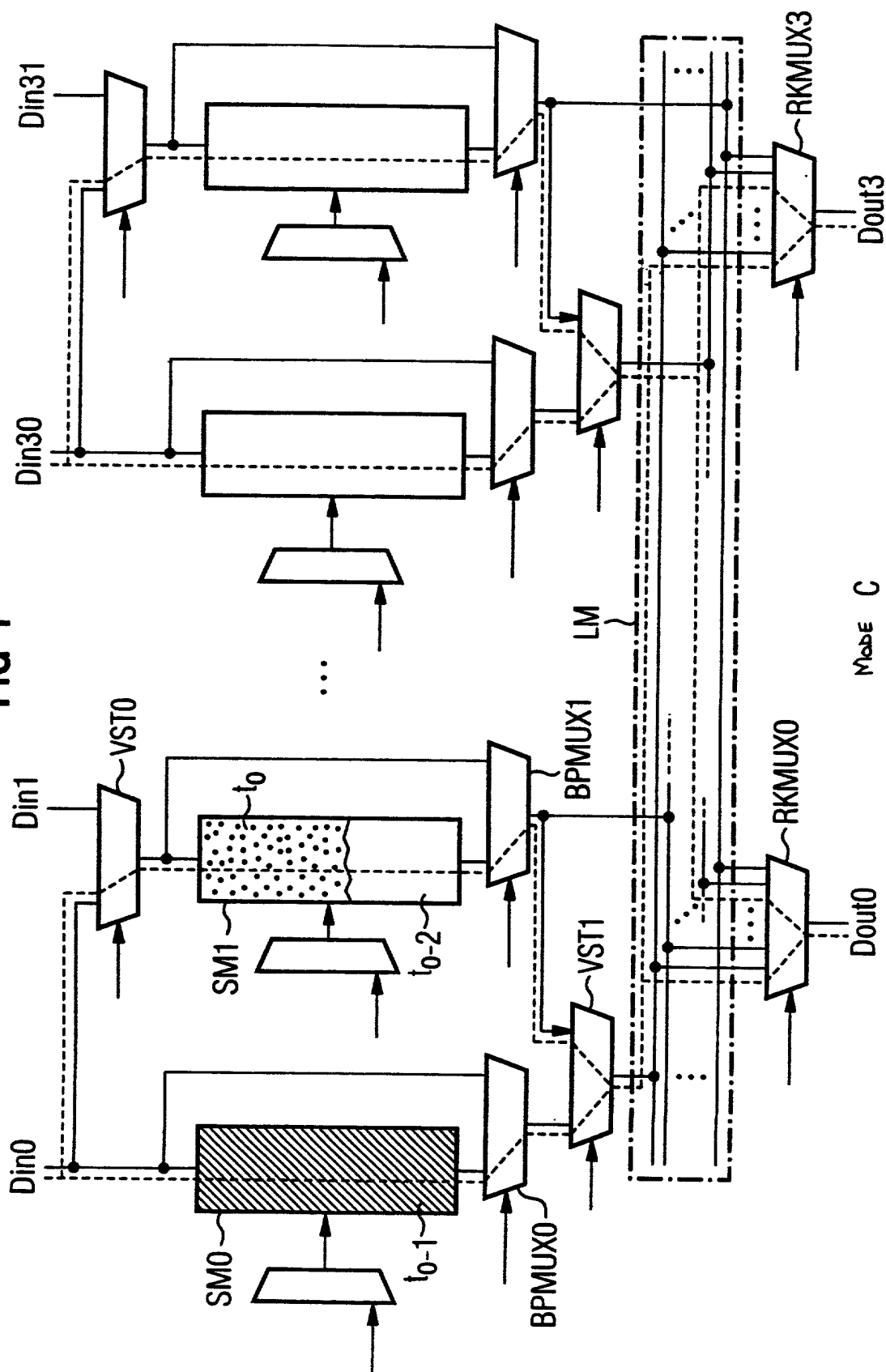


FIG 4

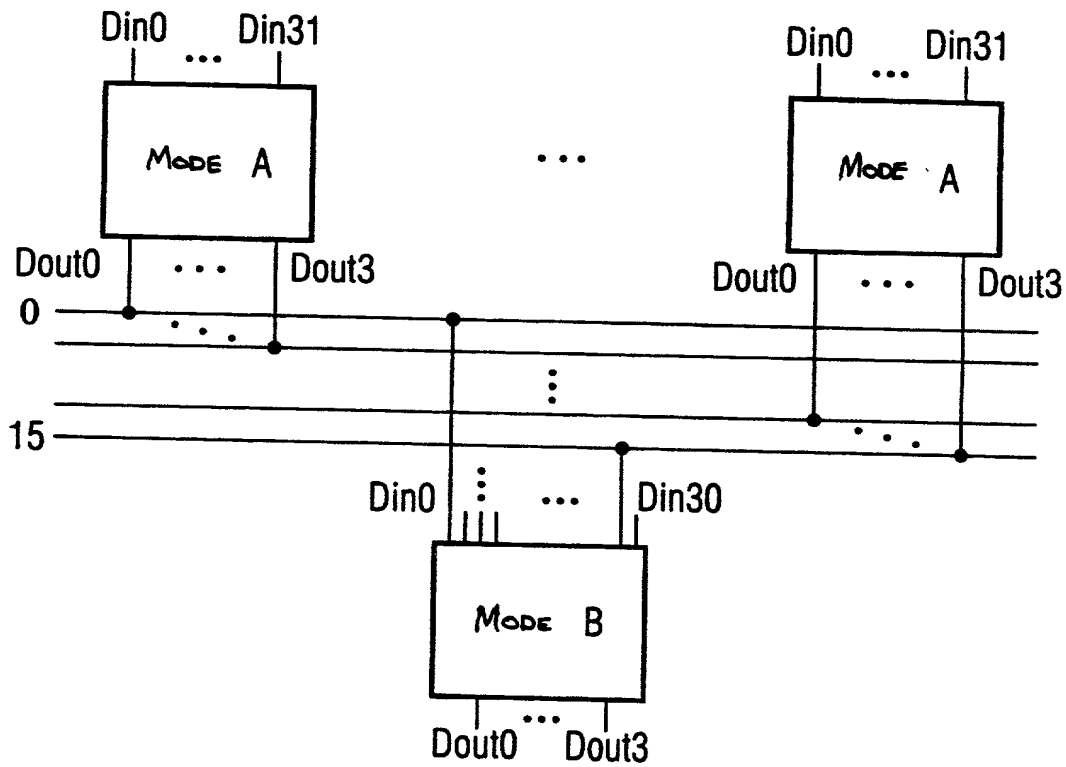


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FIG 5



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